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EXAMINER	
FANG, PAKEE	

ART UNIT	PAPER NUMBER
4146	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/578,822	SMITH ET AL.	
	Examiner	Art Unit	
	PAKEE FANG	4146	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05/09/2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *07/02/2007*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. **Claims 1 – 10 are presented for examination.**

Priority

Acknowledgment is made of applicant's claim for foreign priority & domestic priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in the application filed on 05/09/2006.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 07/02/2007 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, *"a first reference current input", "a second ratioed current input", "a first ratio control input", "a current input",* & *"a second ratio control input"* must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure

must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

Content of Specification

(a) Title of the Invention: See 37 CFR 1.72(a) and MPEP § 606. The title of the invention should be placed at the top of the first page of the specification unless the title is provided in an application data sheet. The title of the invention should be brief but technically accurate and descriptive, preferably from two to seven words may not contain more than 500 characters.

(b) Cross-References to Related Applications: See 37 CFR 1.78 and MPEP § 201.11.

(c) Statement Regarding Federally Sponsored Research and Development: See MPEP § 310.

(d) The Names Of The Parties To A Joint Research Agreement: See 37 CFR 1.71(g).

(e) Incorporation-By-Reference Of Material Submitted On a Compact Disc: The specification is required to include an incorporation-by-reference of electronic documents that are to become part of the permanent United States Patent and Trademark Office records in the file of a patent application. See 37 CFR 1.52(e) and MPEP § 608.05. Computer program listings (37 CFR 1.96(c)), "Sequence Listings" (37 CFR 1.821(c)), and tables having more than 50 pages of text were permitted as electronic documents on compact discs beginning on September 8, 2000.

(f) Background of the Invention: See MPEP § 608.01(c). The specification should set forth the Background of the Invention in two parts:

(1) Field of the Invention: A statement of the field of art to which the invention pertains. This statement may include a paraphrasing of the applicable U.S. patent classification definitions of the subject matter of the claimed invention. This item may also be titled "Technical Field."

(2) Description of the Related Art including information disclosed under 37 CFR 1.97 and 37 CFR 1.98: A description of the related art known to the applicant and including, if applicable, references to specific related art and problems involved in the prior art which are solved by the applicant's invention. This item may also be titled "Background Art."

(g) Brief Summary of the Invention: See MPEP § 608.01(d). A brief summary or general statement of the invention as set forth in 37 CFR 1.73. The summary is separate and distinct from the abstract and is directed toward the invention rather

than the disclosure as a whole. The summary may point out the advantages of the invention or how it solves problems previously existent in the prior art (and preferably indicated in the Background of the Invention). In chemical cases it should point out in general terms the utility of the invention. If possible, the nature and gist of the invention or the inventive concept should be set forth. Objects of the invention should be treated briefly and only to the extent that they contribute to an understanding of the invention.

(h) Brief Description of the Several Views of the Drawing(s): See MPEP § 608.01(f). A reference to and brief description of the drawing(s) as set forth in 37 CFR 1.74.

(i) Detailed Description of the Invention: See MPEP § 608.01(g). A description of the preferred embodiment(s) of the invention as required in 37 CFR 1.71. The description should be as short and specific as is necessary to describe the invention adequately and accurately. Where elements or groups of elements, compounds, and processes, which are conventional and generally widely known in the field of the invention described and their exact nature or type is not necessary for an understanding and use of the invention by a person skilled in the art, they should not be described in detail. However, where particularly complicated subject matter is involved or where the elements, compounds, or processes may not be commonly or widely known in the field, the specification should refer to another patent or readily available publication which adequately describes the subject matter.

(j) Claim or Claims: See 37 CFR 1.75 and MPEP § 608.01(m). The claim or claims must commence on separate sheet or electronic page (37 CFR 1.52(b)(3)). Where a claim sets forth a plurality of elements or steps, each element or step of the claim should be separated by a line indentation. There may be plural indentations to further segregate subcombinations or related steps. See 37 CFR 1.75 and MPEP § 608.01(i)-(p).

(k) Abstract of the Disclosure: See MPEP § 608.01(f). A brief narrative of the disclosure as a whole in a single paragraph of 150 words or less commencing on a separate sheet following the claims. In an international application which has entered the national stage (37 CFR 1.491(b)), the applicant need not submit an abstract commencing on a separate sheet if an abstract was published with the international application under PCT Article 21. The abstract that appears on the cover page of the pamphlet published by the International Bureau (IB) of the World Intellectual Property Organization (WIPO) is the abstract that will be used by the USPTO. See MPEP § 1893.03(e).

(l) Sequence Listing, See 37 CFR 1.821-1.825 and MPEP §§ 2421-2431. The requirement for a sequence listing applies to all sequences disclosed in a given application, whether the sequences are claimed or not. See MPEP § 2421.02.

3. The specification of the disclosure is objected to because the specification lacks section headings for the content of specification as illustrated above. Correction is required. See MPEP § 608.01(b).

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because the abstract repeats information given in the title and include terms such as “said”. Correction is required. See MPEP § 608.01(b).

5. The disclosure is objected to because it contains an embedded hyperlink and/or other form of browser-executable code on page 24 of the specification. Applicant is required to delete the embedded hyperlink and/or other form of browser-executable code. See MPEP § 608.01.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 1- 9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

8. Claims 1 – 9 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: *"a first reference current input", "a second ratioed current input", "a first ratio control input", "a current input", & "a second ratio control input".*

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 – 9 are rejected under 35 U.S.C. 102(e) as being unpatentable over Abe et al. (US Pub.20050024300 A1).

In regard to claim 1, *A current generator for an electroluminescent display driver,* See at least (Abe; Fig. 1) - for organic light emitting luminescent display *"*an organic EL element drive circuit and an organic EL display device using the same organic EL element drive circuit" [0002]

the current generator comprising; See at least (Abe; Fig. 1) - for *"*a reference current generator circuit 1 and a current output circuit 2." [0033]

a first, reference current input to receive a reference current; See at least (Abe; Fig. 1) - for a reference current (Iref) input transistor receives a Iref. "the reference current to drive the input side transistor" [0024]

a second, ratioed current input to receive a ratioed current; See at least (Abe; Fig. 1) - for a rationalize current input means receiving a rationalize current than outputting the current to the next component. "…a plurality of output side transistors for generating output currents to be distributed to a plurality of output pins…" [0024]

a first ratio control input to receive a first control signal input; See at least (Abe; Fig. 1; Item 11) - for a first rationalize current input or transistor receives a drive signal current "a first current mirror circuit including an input side transistor supplied with a predetermined drive current" [0024]

a controllable current mirror having a control input coupled to said first ratio control input, See at least (Abe; Fig. 1) - for a current mirror as an input coupled to the rationalize current control transistor. "A current mirror circuit is constructed with the transistor Qb as an input side transistor" [0011]

a current input coupled to said reference current input, See at least (Abe; Fig. 1) – for the current input mean or transistor of the current (Ir) is coupled to reference current input mean or transistor of the reference current (Iref). "…a P channel MOS FET Trq is connected to the input

side transistor Tra and, together with the transistor Tra, constitute a current mirror circuit…" [0044]

and an output coupled to said ratioed current input; See at least (Abe; Fig. 1) – for the current output mean is coupled to a current input mean or transistor of the rationalize current (Ir). "…a P channel MOS FET Trq is connected to the input side transistor Tra and, together with the transistor Tra, constitute a current mirror circuit…" [0044]

said current generator being configured such that a signal on said control input controls a ratio of said ratioed current to said reference current. See at least (Abe; Fig. 1; Item 11) – for current generator being configured by commands from control circuit which in terms dictates the rationalization for the rationalized current to the reference current in Item 11. "control circuit including an input stage driven by the first current and a certain reference current and an output stage for generating the predetermined drive current corresponding to a difference between the first current and the certain reference current, for controlling the first current in such a manner that the first current becomes substantially equal to the certain reference current by driving the input side transistor by the output stage." [0024]

In regard to claim 2, *further comprising a second ratio control input to receive a second control signal input,* See at least (Abe; Fig. 1; Item 12) – for a second rationalize current input or transistor receives another drive signal current "a first current mirror circuit including an input side transistor supplied with a predetermined drive current" [0024]; Note: "As to the column

driver IC 12, only operational differences thereof from the column driver IC 11 will be described." [0042]

and wherein said ratio of said ratioed current to said reference current is dependent upon a ratio of said first control signal to said second control signal, See at least (Abe; Fig. 1; Item 12) – for a ration of the second rationalize current to the reference current is corresponding to the first control signal from the first driver (item 11) to the second driver (item 12). Please see the output of (Iout to Iin) from Fig. 1. show the rationalize current in Item 12 depends on the first. "a second current corresponding to the output current of said output side transistor of said first current mirror circuit" [Pg. 6; Claim 2]

In regard to claim 3, *wherein said first and second control signals comprise current signals,* See at least (Abe; Fig. 1; Item 12) – for all the circuits are control or drive by current signals "a plurality of current mirror circuits and current-driven by the input currents as shown in FIG. 2."

In regard to claim 4, *further comprising one or more digital to analogue converters to provide said control signal(s);* See at least (Abe; Fig. 1; Item 11 or 12) – for d/a to provide control output signals. "controlled currents Ir are outputted to the respective D/A converter circuits 5 as drive currents and further outputted externally of the column driver IC 11 through the output terminal Iout." [0052]

In regard to claim 5, *comprising a plurality of said ratioed current inputs,* see at least (Abe; Fig. 1; Item 11 or 12) – for a rationalize current input means receiving a rationalize current than outputting the current to the next component. "…a plurality of output side transistors for generating output currents to be distributed to a plurality of output pins…" [0024]

and a corresponding plurality of said second ratio control inputs for setting a plurality of said current ratios, see at least (Abe; Fig. 1; Item 11 or 12) – for a rationalize current input means rationalizing the current into different current components. "…a plurality of output side transistors for generating output currents to be distributed to a plurality of output pins…" [0024]

one for each of said second ration control inputs. See at least (Abe; Fig. 1; Item 11 or 12) – for a second rationalize current input or transistors having one current (Ir) per input or transistors.

In regard to claim 6, *further comprising a plurality of drive connections,* See at least (Abe; Fig. 1; Item 11 or 12) – for a plurality of drivers and drive connections. "the number of column IC drivers is three currently and the number of terminal pins of each driver for one of R, G and B display colors" [0007] & "Output currents i of the transistors Q1 to Qm of the drivers are supplied to the pins through the switches S1 to Sm and output terminals X1 to Xm," [0009]

and a selector to select one of said drive connections as said reference current input and another of said drive connections as said ratioed current input. See at least (Abe; Fig. 1; Item 11 or 12;

Item SW1, SW2) – for a selector to select on the drive connections for the reference current and other connection for the rationalized current input. "The switches SW1 and SW2 and the inverter 3b constitute a selector circuit for selecting either one of the currents from the input terminal Iin and the reference current Iref generated by the reference current source 3a." [0040]

In regard to claim 7, *wherein said selector is coupled to said drive connections to selectively couple a selected one of said drive connections to said reference current input and another of said drive connections to said ratioed current input.* See at least (Abe; Fig. 1; Item 11 or 12; Item SW1, SW2) – for a selector that is couple to the drive connections to selectively couple to a selected one of the connections to the reference current and other connection for the rationalized current input. "The switches SW1 and SW2 and the inverter 3b constitute a selector circuit for selecting either one of the currents from the input terminal Iin and the reference current Iref generated by the reference current source 3a." [0040]

In regard to claim 8, *wherein said current mirror comprises a plurality of mirror units, one for each of said plurality of drive connections,* See at least (Abe; Fig. 1; Item 11 or 12; Items trp, trc, trn, etc) – for a current mirror comprises many mirror units, one for each of the drive connections. " first current mirror circuit including an input side transistor supplied with a predetermined drive current and a plurality of output side transistors for generating output currents to be distributed to a plurality of output pins provided correspondingly to terminal pins of an organic EL pa"el" [0024]

and wherein said selector is configured to selectively couple at least said first ratio control input to a said mirror unit. See at least (Abe; Fig. 1; Item 11 or 12; Items SW1, SW2) – for a selector which is configured to selectively couple to at least a control transistor to the mirror unit. "current mirror circuit and said output transistor of said second current mirror circuit when said selector selects the third current." (Page 7, Claim 7)

In regard to claim 9*, An OLED display driver comprising a current generator for an electroluminescent display driver,* See at least (Abe; Fig. 1) - for organic light emitting luminescent display *"*an organic EL element drive circuit and an organic EL display device using the same organic EL element drive circuit" [0002]

the current generator comprising: See at least (Abe; Fig. 1) - for *"*a reference current generator circuit 1 and a current output circuit 2." [0033]

a first, reference current input to receive a reference current; See at least (Abe; Fig. 1) - for a reference current (Iref) input transistor receives a Iref. *"*the reference current to drive the input side transistor" [0024]

a second, ratioed current input to receive a ratioed current; See at least (Abe; Fig. 1) - for a rationalize current input means receiving a rationalize current than outputting the current to the next component. "…a plurality of output side transistors for generating output currents to be distributed to a plurality of output pins…" [0024]

a first ratio control input to receive a first control signal input; See at least (Abe; Fig. 1; Item 11) - for a first rationalize current input or transistor receives a drive signal current "a first current mirror circuit including an input side transistor supplied with a predetermined drive current" [0024]

a controllable current mirror having a control input coupled to said first ratio control input, See at least (Abe; Fig. 1) - for a current mirror as an input coupled to the rationalize current control transistor. "A current mirror circuit is constructed with the transistor Qb as an input side transistor" [0011]

a current input coupled to said reference current input, See at least (Abe; Fig. 1) – for the current input mean or transistor of the current (Ir) is coupled to reference current input mean or transistor of the reference current (Iref). "…a P channel MOS FET Trq is connected to the input side transistor Tra and, together with the transistor Tra, constitute a current mirror circuit…" [0044]

and an output coupled to said ratioed current input; See at least (Abe; Fig. 1) – for the current output mean is coupled to a current input mean or transistor of the rationalize current (Ir). "…a P channel MOS FET Trq is connected to the input side transistor Tra and, together with the transistor Tra, constitute a current mirror circuit…" [0044]

said current generator being configured such that a signal on said control input controls a ratio of said ratioed current to said reference current. See at least (Abe; Fig. 1; Item 11) – for current generator being configured by commands from control circuit which in terms dictates the rationalization for the rationalized current to the reference current in Item 11. "control circuit including an input stage driven by the first current and a certain reference current and an output stage for generating the predetermined drive current corresponding to a difference between the first current and the certain reference current, for controlling the first current in such a manner that the first current becomes substantially equal to the certain reference current by driving the input side transistor by the output stage." [0024]

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 10 are rejected under 35 U.S.C. 102(b) as being unpatentable over Routley (GBP 85906).

In regard to claim 10, *A current driver circuit for driving a plurality of electrodes of an electroluminescent display, said driver circuit comprising;* See at least (Routley; Fig. 9; Item 510 & 512) – for current drivers circuits for driving electrodes of an electroluminescent display. "a

display diver providing a controlled current drive." [Page 1 abstract] & "a display driver control circuitry for a passive matrix electroluminescent display, the display comprising a plurality of pixels arranged in rows and columns and addressed by row and column electrodes" [0035]

a control input to receive a control signal; See at least (Routley; Fig. 9) – for "current control input 410 is provided to current driver block 406 and, for the purposes of illustration, this is shown connected to the base of transistor 416 although in practice a current mirror arrangement is preferred. The signal on current controlline 410 may comprise either a voltage or a current signal and this is preferably provided from a digital-to-analogue converter (not shown in FIG. 4b) for ease of interfacing" [0050]

a plurality of drive connections for said plurality of display electrodes; See at least (Routley; Fig. 9) – for a drive connections for many display electrodes.

a selector configured to select one of said plurality of drive connections as a first connection, See at least (Routley; Fig. 9 Item 512a) – for a selector configured to select at least one of the drive connections as a first connection of the row 1 of the electrode.

and at least one other of said drive connections as a second connection; See at least (Routley; Fig. 9 Item 512a) – for a selector (Item 512a) configured to select at least one of the drive connections as a second connection of the row 2 of the electrode.

and a driver configured to provide respective first and second drive signals for said first and second connections, See at least (Routley; Fig. 9 Item 512a) – for driver configured to provide drive signals for all of the connections. "a display driver circuitry for driving a matrix of electroluminescent display elements, the display elements being addressed by first and second pluralities of respective first and second electrodes, the display driver circuitry comprising first display interface circuitry for interfacing to said first electrodes; second display interface circuitry for interfacing to said second electrode; control circuitry coupled to said first display interface circuitry and to said second display interface circuitry and configured to control said first and second display interface circuitry to activate successive sets of said display elements by activating successive ones of said first electrode in combination with a set of said second electrode;" [0035]

a ratio of said first and second drive signals being controlled in accordance with said control signal. See at least (Routley; Fig. 9) – for a driver inputs a control signal with dictates the severity of all the current output of the drive signal. "driver 510 also have a control input 517 for setting a reference current drive level, for use by the individual column drivers. Thus, for example, control input 517 may provide a control signal for a reference current (or voltage) generator supplying a reference current (or voltage) to a digital-to-analogue converter or converters providing current control signals to current drivers for the individual columns." [0055] & "circuitry 510 includes a controllable reference current source 604 controlled by an input signal on control line 517 and providing a reference current output on line 606 used," [0066]

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to PAKEE FANG whose telephone number is (571)270-7219. The examiner can normally be reached on Monday-Friday 9AM-5PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patel Ramesh can be reached on (571)272-3688. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/PAKEE FANG/

Examiner, Art Unit 4146

/Ramesh B. Patel/

Supervisory Patent Examiner, Art Unit 4146